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<u>L32</u>	L26 and 19	39	<u>L32</u>
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<u>L29</u>	L26 and 16	5	<u>L29</u>
<u>L28</u>	L26 and 15	15	<u>L28</u>
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<u>L26</u>	116 and instruction\$1 near6 decod\$4	198	<u>L26</u>
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<u>L25</u>	L24 and 116	110	<u>L25</u>
<u>L24</u>	(710/22,23)[CCLS]	1454	<u>L24</u>

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<u>L23</u>	L17 and I9	128	<u>L23</u>
<u>L22</u>	L17 and I8	2	<u>L22</u>
<u>L21</u>	L17 and I7	50	<u>L21</u>
<u>L20</u>	L17 and I6	50	<u>L20</u>
<u>L19</u>	L17 and I5	15	<u>L19</u>
<u>L18</u>	L17 and I4	54	<u>L18</u>
<u>L17</u>	L16 and (integrated or chip or semiconductor or monolithic)	808	<u>L17</u>
<u>L16</u>	(gp or general near1 purpose near1 register\$1) near55 (dma or direct near1 memory near1 access\$3) and (reconfigur\$6 or configur\$6 or extension\$3 or extend\$5)	1355	<u>L16</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L15</u>	I3 and I9	126	<u>L15</u>
<u>L14</u>	I3 and I8	2	<u>L14</u>
<u>L13</u>	I3 and I7	220	<u>L13</u>
<u>L12</u>	I3 and I6	220	<u>L12</u>
<u>L11</u>	I3 and I5	254	<u>L11</u>
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<u>L9</u>	(710/22-74)[CCLS]	11861	<u>L9</u>
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<u>L7</u>	(711/112-173)[CCLS]	25652	<u>L7</u>
<u>L6</u>	(711/112-173)![CCLS]	25652	<u>L6</u>
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<u>L4</u>	(712/2-300)[CCLS]	13389	<u>L4</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2 and instruction\$1 near6 decod\$4	1882	<u>L3</u>
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<u>L1</u>	(gp or general near1 purpose near1 register\$1) and (dma or direct near1 memory near1 access\$3) and (reconfigur\$6 or configur\$6 or extension\$3 or extend\$5)	22343	<u>L1</u>

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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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☐ 1. A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, : decoder

Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba, A.; Yamamoto, Y.; F. M.; Yutaka, T.; Okada, T.; Nagamatsu, M.; Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashi Murakami, H.; Ohtaguro, Y.; Aono, A.;

[Solid-State Circuits, IEEE Journal of](#)

Volume 34, Issue 11, Nov. 1999 Page(s):1608 - 1618

Digital Object Identifier 10.1109/4.799870

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☐ 2. A236 parallel DSP chip provides real-time video processing economically and efficiently Morton, S.G.;

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Digital Object Identifier 10.1109/ELECTR.1996.501237

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Miyagoshi, E.; Araki, T.; Sayama, T.; Ohtani, A.; Minemaru, T.; Okamoto, K.; Kodama, H.; Morishig Aoki, K.; Mitsumori, T.; Imanishi, H.; Jinbo, T.; Tanaka, Y.; Taniyama, M.; Shingou, T.; Fukumoto, T. K.;

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Cates, R.L.; Farrell, J.J., III;

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**5. CPU for PlayStation(R)2**

Tago, H.; Hashimoto, K.; Ikumi, N.; Nagamatsu, M.; Suzuki, M.; Yamamoto, Y.;

Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings

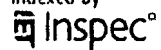
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